PRELIMINARY - REVERSED ENGINEERED

**Lionel E-Unit
00-0103-00
Theory of Operation**

**Revision A
05 FEB 2015**

Revision History

Revision	Date	By	Description
-	19 JAN 2015	Paul Romsky	Initial Release
A	05 FEB 2015	Paul Romsky	Added Original Designer Section

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List of Equations
There are no equations in this document at this time

1. Overview

Notice: The terms used here are for individuals with an electronics background, it is not intended for a wider audience.

The E-Unit is a small (approximately 25 mm x 50 mm x 15 mm) single layer Printed Circuit Board (PCB) that controls a Lionel locomotive Direct Current (DC) motor direction by detecting brief drop-outs in power (as when the Direction button is pressed on an external Track Transformer).

There are four states of the E-Unit:
Forward, Neutral, Reverse, Neutral

Note: Sometimes the E-Unit is referred to as a 3-State switch (Forward, Neutral, and Reverse) because these are the states the casual user sees.

Although there is no apparent difference in the two Neutral states functionally, they are two distinct states electronically.

After long durations without power, a built-in Power-On Reset (POR) circuit will place the E-Unit in the first state (Forward).

The E-Unit has the following sections of circuitry:
Input Power
Logic Supply
Power Interrupt Detector
Direction Logic
Motor Switch

1.1   Original Designer

It has been reported that the E-Unit design (implemented by Lionel in this case) was based on an original design published in a 1970's era model train magazine. When a reference to that article can be made, credit of the original design will be given to that author. This document was created in that same spirit of free exchange of ideas - to further the interest in the model train hobby and similar industry.

2. Electro-Static Discharge

This section provides information on Electro-Static Discharge concerns.

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WARNING

Handle the E-Unit only at a
Static Free workstation

</div>

The components used on the E-Unit are susceptible to Electro-Static Discharge (ESD) and can be damaged by simple handling. Mild static energy (even seemingly undetectable) can damage these components. The microcircuit (chip) on the E-Unit is a CMOS device and is especially susceptible to ESD damage.

3. Specifications

The physical and operating specifications for the E-Unit are shown in Table 1.

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Table 1 - Specifications

</div>

Parameter	Description
Manufacturer	Lionel
Part Number	00-0103-00
Price	Estimated $15.00 USD MSRP ca. 1980
Dimensions (Overall)	50 mm x 25 mm x 15 mm (L x W x H)
Weight	75 g (Max)
Input Voltage	8 VAC RMS to 20 VAC RMS -or- 8 VDC to 20 VDC
Input Current	1 A (Max)
Output Voltage	8 VAC RMS to 20 VAC RMS –or- 8 VDC to 20 VDC
Output Current	1 A (Max)
Power Dissipation (Neutral)	100 mW (Typical)
Power Dissipation (Full Load)	2.5 W (Max)
Operating Temperature (Ambient)	0º C to 28˚C
Storage Temperature	-40º C to 55º C
Humidity Storage/Operating (Non-Condensing)	30% to 70%
Altitude Storage/Operating	0 to 3Km Above MSL
Salt Mist (Corrosive Atmosphere)	None – Not recommended for marine or coastal use
Explosive Atmosphere	None Allowed
Shock/Vibration	2 G (Max) X, Y, and Z Axis
PCB Material	FR-4 Substrate, Single Copper Layer
PCB Traces	1 oz Copper (Cu)
Solder	60% Tin / 40% Lead (Sn/Pb)
Flux	No Clean Liquid Flux NC-264-5
Conformal Coating	None
Stenciling	Silk Screen (Green Ink)

4. Electrical Interface

The E-Unit has a four wire interface, See Table 2:

Table 2 - External Connections

Signal	Direction	Reference Designator	Wire Color	Function
ACHOT	Input	W2	Grey	From Center Rail Pick-Up
ACGND	Input	W1	Brown	From Outer Rails Pick-Up
MOTP	Output	W4	Red	To Motor Positive Terminal
MOTN	Output	W3	Black	To Motor Negative Terminal

5. Parts List

The components used on the E-Unit PCB are shown in Table 3. Note: The part numbers were determined by reverse engineering and may not be the actual parts in the design (but are compatible). This was due to poor readability of the markings on most components used on the subject E-Unit used in the reverse engineering process. See Figure 1 for each component's placement on the PCB (A1).

Table 3 - Parts List

Reference Designators	Part Number	Qty	Description
A1		1	Circuit Board, Printed, E-Unit (Mfr: Lionel)
C6		1	Capacitor, Mylar, 0.001uF, 50WVDC, Tol +/-10%
C1, C3, C5		3	Capacitor, Electrolytic, 1uF, Polarized, 50WVDC, Tol +/-

			10%
C4		1	Capacitor, Electrolytic, 4.7uF, Polarized, 50WVDC, Tol +/- 10%
C2		1	Capacitor, Electrolytic, 100uF, Polarized, 25WVDC, Tol +/-10%
CR1-CR5	1N4001	5	Diode, Power, 1A
CR7-CR12	1N4148	6	Diode, Signal
CR6	1N5239	1	Diode, Zener, 9.1V
Q1-Q2	TIP31	2	Transistor, Power, NPN, TO-220 Pkg
Q3-Q4	TIP32	2	Transistor, Power, PNP, TO-220 Pkg
Q5-Q7	MPSA13	3	Transistor, Darlington, NPN, TO-93 Pkg
R1-R3, R7		4	Resistor, Carbon, 15 Ohm, 0.25W, Tol +/-10%
R5		1	Resistor, Carbon, 10K Ohm, 0.25W, Tol +/-10%
R4, R6		2	Resistor, Carbon, 22K Ohm, 0.25W, Tol +/-10%
R8, R12		2	Resistor, Carbon, 58K Ohm, 0.25W, Tol +/-10%
R9-R10		2	Resistor, Carbon, 100K Ohm, 0.25W, Tol +/-10%
R11		1	Resistor, Carbon, 220K Ohm, 0.25W, Tol +/-10%
U1	CD4013BCN	1	Microcircuit, Dual Flip/Flop, Positive Clk, Complementary Outputs, Async Positive Set/Reset, Plastic DIP-14 (Mfr: National Semiconductor)
W1		1	Wire, 24 AWG, Stranded Cu, Brown, Plastic Sheath, 200 mm
W2		1	Wire, 24 AWG, Stranded Cu, Grey, Plastic Sheath, 200 mm
W3		1	Wire, 24 AWG, Stranded Cu, Black, Plastic Sheath, 200 mm
W4		1	Wire, 24 AWG, Stranded Cu, Red, Plastic Sheath, 200 mm

6. Input Power

This section (see Figure 1 and Figure 2) consists of four diode rectifiers (CR1, CR2, CR3 and CR4) arranged in a Full-Wave Bridge. The Full-Wave Bridge converts the AC inputs: ACHOT (W2), and ACGND (W1), into a full wave DC (high ripple) signal (FWRECDC) from the Positive (+) output of the bridge with respect to the negative (-) output of the bridge, which is Ground (GND). The AC Input voltages are typically anywhere from 8 VAC RMS to 20 VAC RMS (depending on the external Track Transformer throttle position). 8 VDC to 20 VDC can also be used to supply the E-Unit as the Full-Wave Bridge inherently allows for this. The FWRECDC signal provides power to the Logic Supply, Power Interrupt Detector, and the Motor Switch circuitry.

7. Logic Supply

This section (see Figure 1 and Figure 2) creates the supply voltage (VCC) to the Direction Logic and a bias voltage for the Power Interrupt Detector circuitry. FWRECDC passes through an isolation diode (CR7) so that the FILTDC signal can be created by the 100uF capacitor (C2). This capacitor has two functions, first to filter the high DC ripple of the FWRECDC signal into a smooth DC voltage. Second, this capacitor acts as a Hold-Up supply to keep VCC constant during power drop-outs (for instance when commanding the E-Unit to change states). The load of the VCC signal is so low that this capacitor can keep VCC constant for several minutes. The FILTDC signal is passed to a Zener Current Limiting resistor (R5) and a 9.1 V Zener Diode (CR6). This arrangement shunt regulates the smooth FILTDC voltage (which can be anywhere between 11 VDC and 28 VDC depending on the filtering action of the AC input voltage) down to a constant 9.1 VDC to become the Supply Voltage for other circuitry (VCC). A

decoupling capacitor (C1) is provided from VCC to GND to reduce switching noise from the Direction Logic circuitry.

8. Power Interrupt Detector

This section (see Figure 1 and Figure 3) creates a positive going pulse when the AC input power is briefly dropped (about 1 second) and then restored. FWRECDC passes through an isolation diode (CR8) so that the TRIGDCFILT signal can be created by the Low Pass Filter (R4 and C3). This Low Pass Filter "smooths" the high DC ripple of the FWRECDC signal into a steady DC voltage.

When AC input power is present, the TRIGDCFILT signal will be anywhere between 11 VDC and 28 VDC depending on the filtering action of the AC input voltage. This voltage is passed through a Base Current Limiter resistor (R6) and saturates the B-E junction of Threshold Detector/Inverter (Q5) Darlington transistor. In this condition, the C-E pins of Q5 will conduct and 0V will be present on the Trigger signal (TRIG).

When AC input power is interrupted, the TRIGDCFILT signal will rapidly decay to 0V, thereby cutting off the B-E junction of Q5. In this condition the C-E pins of Q5 will not conduct (high impedance), and VCC (9.1 VDC) will be provided to the TRIG signal via the Inverter Load Resistor (R8). A Transient Filter (C5) is provided across the TRIG signal and GND to eliminate triggers from very short (< 1 second) drop-outs (as when AC power may be interrupted as the locomotive moves along a track). The TRIG signal is sent to the Direction Logic circuitry to advance the state of E-Unit.

9. Direction Logic

This section (see Figure 1 and Figure 3) consists primarily of a two-bit binary counter (4 condition state machine) implemented in a Dual D-Type Flip/Flop (U1). Each Flip/Flop is configured as a digital Toggle Flip/Flop. The Flip/Flops are powered by VCC (which remains constant even during AC input power drop-outs). A Power-On Reset Circuit (C4 and R12) is a simple differentiator that will generate a short pulse (RESET) which is sent to the Reset Inputs (R) on each Flip/Flop. The pulse will only be generated if the AC input power is off for a substantially long period of time (on the order of several minutes - when VCC decays to near 0V). The RESET signal places both Flip/Flops in Reset (Forward state).
The Run/Neutral Flip/Flop (1st stage) feeds its Complement output Q Not (U1 pin 12) through an Integrator (R11 and C6) to its Data input (U1 pin 9). This allows the Flip/Flop to operate as a toggle Flip/Flop. The Integrated signal (DATAB) prevents multiple triggering and meta-stability (in event of noise) of the Q1-B Flip/Flop by improving setup time and slowing down (rounding off) the edges from the Q Not output (U1 pin 12). The Forward/Reverse Flip/Flop (2nd stage) simply feeds its Complement output Q Not (U1 pin 2) to its Data input (U1 pin 5) with no integrator needed as this is accomplished by the 1st stage. Again, this allows this Flip/Flop to operate as a toggle Flip/Flop as well.

 When AC input power is dropped briefly (about 1 second) the TRIG signal (from the Power Interrupt Detector circuitry) will pulse high then low (present at the Clock input U1 pin 11) and the rising edge will toggle the Run/Neutral Flip/Flop (U1-B) to the next state. When the Run/Neutral Flip/Flop Q Not (U1 pin 12) goes high, the next stage (U1-A) is toggled due to the signal being connected (cascaded) to the U1-B clock input (Q1 pin 3), this in effect creates a two-bit binary counter.

The Run/Neutral Flip/Flip Q Not output (U1 pin 12 - RUN) goes high (RUN) when a Non-Neutral state is selected. This high signal will prime one, but not completely satisfy both of the AND gates of the H-Bridge in the Motor Switch circuitry.

The Run/Neutral Flip/Flip Q Not output (U1 pin 12 - RUN) goes low (NEUTRAL_N, read as Neutral Not) when the Neutral state is selected. This low signal disables both AND gates (in the Motor Switch circuitry) and thus disables the H-Bridge (the Neutral or Motor Off state). The Run/Neutral Flip/Flip Q output (U1 pin 13) is not used in this implementation and is left Not Connected (NC).

The Forward/Reverse Flip/Flop Q Not output (U1 pin 2 - FWD) goes high when in the Forward states. The Forward/Reverse Flip/Flop Q output (U1 pin 1 - REV) goes high when in the Reverse states. These two signals are complementary and both cannot be high or be low at the same time (if one is high the other is low).

The Set inputs (S) of each Flip/Flop are tied to GND since the Pre-Set feature of the Flip/Flops are not used in this implementation.

The states of the Direction Logic are as follows, see Table 4.

Table 4 - Direction States

| State | Count | Flip/Flop (Stage) | | Function |
		U1-B (Stage 1) Run/Neutral	U1-A (Stage 2) Forward/Reverse	
1	0	Reset	Reset	Forward (Power-On Reset State)
2	1	Set	Reset	Neutral
3	2	Reset	Set	Reverse
4	3	Set	Set	Neutral
After State 4, the State cycles back to State 1				

10.   Motor Switch

This section (see Figure 1 and Figure 4) consists primarily of four transistors (Q1, Q2, Q3, and Q4) arranged in a H-Bridge. The H-Bridge is an electronic implementation of a Double-Pole/Double-Throw (DPDT) switch with Center Off. Resistors (R1, R2, R3, and R7) limit the current trough the Base of each transistor (Q4, Q1, Q3 and Q2) respectively to allow saturation without overdriving the transistors.

FWRECDC passes through an isolation diode (CR5) so that the H-Bridge Power (HBDC) does not feed back to other circuitry. There is no filtering of the HBDC signal as a DC motor can operate normally on a full wave rectified (high ripple) DC signal - essentially spinning to the RMS resulting DC voltage of the full wave DC signal.

A Diode AND Gate (R10, CR10, and CR11) is implemented for the Forward gating function and another Diode AND Gate (R9, CR9, and CR12) is implemented for the Reverse gating function. When in the Neutral state, RUN will be low, this will dissatisfy both AND Gates (thus 0V will be on both the FWDG and REVG signals).

When not in the Neutral state (Run state), RUN will be high. With RUN high and if the state is Forward, the FWD signal will be high (REV will be low). This will satisfy only the Forward AND Gate, thus HBDC

will be present on the FWDG signal. This will bias the B-E junction of the Forward Driver Darlington Transistor (Q7). Saturating current will flow through the E-B junction of Q1 (HBFNB), through R1 (HBFWDN), through the E-C of Q7 (HBFWDP), through R2 (HBFPB), and through the B-E junction of Q4. With Q1 saturated, GND will be provided (via Q1 E-C pins) on the MOTN (W3) signal, and with Q4 saturated, HBDC will be provided (via Q4 E-C pins) on the MOTP (W4) signal, thus causing the external DC motor to spin in the Forward direction in proportion to the RMS voltage of HDBC.

With RUN high and if the state is Reverse, the REV signal will be high (FWD will be low). This will satisfy only the Reverse AND Gate, thus HBDC will be present on the REVG signal. This will bias the B-E junction of the Reverse Driver Darlington Transistor (Q6). Saturating current will flow through the E-B junction of Q2 (HBRNB), through R3 (HBREVN), through the E-C of Q6 (HBREVP), through R7 (HBRPB), and through the B-E junction of Q3. With Q2 saturated, GND will be provided (via Q2 E-C pins) on the MOTP (W4) signal, and with Q3 saturated, HBDC will be provided (via Q3 E-C pins) on the MOTN (W3) signal, thus causing the external DC motor to spin in the Reverse direction in proportion to the RMS voltage of HDBC.

Note: Due to the arrangement of the H-Bridge transistors, the Tabs (Collector - heat sinks) on Q1 and Q3 may touch each other, and the Tabs (Collector - heat sinks) on Q2 and Q4 may touch each other, no other tab combinations may touch (else a short circuit will occur). However, it is best to leave a large air gap between all of these transistor tabs for better heat dissipation.

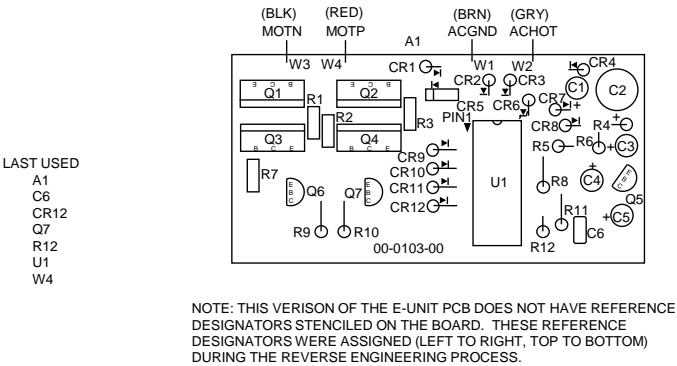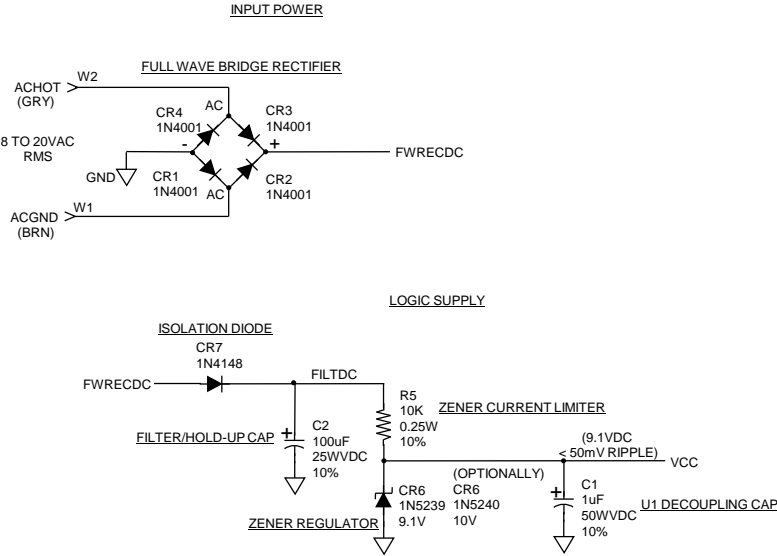**PRELIMINARY - REVERSED ENGINEERED**

Layout

Figure 1 - PCB Layout

INPUT POWER

Figure 2 - Schematic Page 1

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Figure 3 - Schematic Page 2

Figure 4 - Schematic Page 3

11.   Acronyms

This section lists all acronyms used in this document. This may contain acronyms that are not mentioned in this document but are related to other acronyms in this document.

Terms:

-A	Sub Component A of a multiple component device (in a Reference Designator Context)
-B	Sub Component B of a multiple component device (in a Reference Designator Context)
A	Amperes, or Amps (In an Electrical Current context)
A	Assembly (in a Reference Designator context)
AC	Alternating Current
AND	Logic Function were all inputs must be satisfied for the output to be active
Async	Asynchronous
AWG	American Wire Gauge
B	Base (in a Transistor Context)
C	Capacitor (in a Reference Designator context)
C	Collector (in a Transistor context)
C	Celsius (in a Temperature context)
ca.	Circa
Cu	Copper
CLK	Clock (or Clk)
CMOS	Complementary Metal Oxide Semiconductor
CR	Crystal Rectifier (Diode)
DIP	Dual In-Line Package (a device package, usually a dash and the number of pins follow)
DC	Direct Current
DPDT	Double-Pole/Double-Throw (also known as a 4-way switch)
E	Emitter (in a Transistor context)
ESD	Electro-Static Discharge
E-Unit	Lionel Electronic Switch Unit (not to be confused with an E-Switch Track section)
F	Farad (a unit of Capacitance)
F/F	Flip/Flip (Bi-Stable Multi-Vibrator)
FR-4	Flame Retardant Material 4
FW	Full Wave
g	Grams
G	G Force
GND	Ground (0V Reference)
H-BRIDGE	Four Transistors arranged so that a DPDT switch is implemented electronically
k	Lowercase K (kilo = 1×10^{3}) Sometimes shown as Uppercase K
m	Lowercase M (milli = 1×10^{-3})
mm	Millimeter (1×10^{-3} Meters)
Mfr	Manufacturer
MSL	Mean Sea Level
MSRP	Manufacturer's Suggested Retail Price
NOT	A Complementary (opposite) Logic Level (or an Active Low logic Level)
NPN	Negative-Positive-Negative
oz	Ounce (weight)
OR	Logic Function were one or more inputs must be satisfied for the output to be active
PCB	Printed Circuit Board
Pb	Lead
POR	Power-On Reset
Pkg	Package
PNP	Positive-Negative-Positive
Q	Transistor (in a Reference Designator context)
Q	True Output of a Flip/Flop
Q Not	Q_N, Q Not, or Q with a vinculum (bar) above – Complement Output of a Flip/Flop
R	Resistor (in a Reference Designator context)
R	Reset Pin of Flip/Flop (in a Logic context)
RMS	Root Mean Squared (the effective resulting DC voltage of a sine or full wave signal)
S	Set Pin of a Flip/Flop (in a Logic context)
Sn	Tin
SW	Switch
TO	Transistor Outline
Tol	Tolerance

u	Lowercase U, representing the Lowercase Greek Letter Mu (μ) (micro = 1 x 10^{-6})
U	Microcircuit (in a Reference Designator context)
USD	United States Dollars
V	Volts (in an Electrical Potential context)
VAC	Volts AC
VCC	Voltage Collector Supply (Digital Logic Voltage)
VDC	Volts DC
W	Wire (or Cable) (in a Reference Designator context)
W	Watts (in an Electrical Power context)
WVDC	Working Volts DC
X	A Horizontal (Left/Right) Axis (in a Direction context)
Y	A Horizontal (Front/back) Axis (in a Direction context)
Z	The Vertical (up/Down) Axis (in a Direction context)
Z	Impedance (in an Electrical Reactance context)
Ω	Uppercase Greek Letter Omega (Ohms, a unit of Resistance)

Signals: (all active high unless otherwise indicated)

ACHOT	AC Hot
ACGND	AC Ground
DATAB	Data Input B
FILTDC	Filtered Direct Current
FWD	Forward
FWDG	Forward Gate
FWRECDC	Full Wave Rectifier Direct Current
HBDC	H-Bridge Direct Current
HBFWDN	H-Bridge Forward Negative
HBFWDP	H-Bridge Forward Positive
HBFNB	H-Bridge Forward Negative Base
HBFPB	H-Bridge Forward Positive Base
HBREVN	H-Bridge Reverse Negative
HBREVP	H-Bridge Reverse Positive
HBRNB	H-Bridge Reverse Negative Base
HBRPB	H-Bridge Reverse Positive Base
MOTN	Motor Negative
MOTP	Motor Positive
NEUTRAL_N	Neutral Not – Active Low (not in Run)
RESET	Power-On Reset Signal
REV	Reverse
REVG	Reverse Gate
RUN	Run – Active High (not in Neutral)
TRIG	Trigger
TRIGB	Trigger Base
TRIGDCFILT	Trigger DC Filtered
VCC	Digital Logic Supply Voltage (Voltage Collector Supply)

Colors (Value):

BLK	Black	(0)
BRN	Brown	(1)
RED	Red	(2)
ORN	Orange	(3)
YEL	Yellow	(4)
GRN	Green	(5)
BLU	Blue	(6)
VIO	Violet	(7)
GRY	Grey	(8)
WHT	White	(9)

12.   Index

There is no Index for this document at this time.

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